AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1 (original): An electroplating process comprising electroplating an electrically conductive substrate wherein the electroplating is performed intermittently using said substrate surface as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

2 (original): The electroplating process according to Claim 1 wherein said intermittent electroplating is performed by repeating application of a voltage between a cathode and an anode and interruption of said application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

3 (original): A process for producing a circuit board comprising a substrate and, as formed thereon, a conductor circuit by electroplating which is performed intermittently using the electrically conductive conductor circuit-forming surface as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

4 (original): The process for producing a circuit board according to Claim 3 wherein said intermittent electroplating is performed by repeating application of a

voltage between a cathode and an anode and interruption of said application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

5 (original): A process for manufacturing a printed circuit board which comprises disposing a resist on an electrically conductive layer formed on a substrate, performing electroplating, stripping the resist off and etching said electrically conductive layer to provide a conductor circuit, wherein the electroplating is performed intermittently using said electrically conductive layer as cathode and a plating metal as cathode at a constant voltage between said anode and said cathode.

6 (original): A process for manufacturing a printed circuit board which comprises disposing an interlayer resin insulating layer on a substrate formed with a conductor circuit, creating openings for formation of via holes in said interlayer resin insulating layer, forming an electroless plated metal layer on said interlayer resin insulating layer, disposing a resist thereon, performing electroplating, stripping the resist off and etching the electroless plated metal layer to provide a conductor circuit and via holes, wherein the electroplating is performed intermittently using said electroless plated metal layer as cathode and a plating metal as anode at a constant voltage between said anode and said cathode.

7 (original): The process for manufacturing a printed circuit board according to Claim 6 wherein said interlayer resin insulation layer has a metal layer on its surface.

8 (original): The process for manufacturing a printed circuit board according to Claim 5, 6 or 7 wherein said intermittent electroplating is performed by repeating application of a voltage and interruption of application alternately with a voltage time/interruption time ratio of 0.01 to 100, a voltage time of not longer than 10 seconds and an interruption time of not less than $1x10^{-12}$ seconds.

Claims 9-13: (canceled).

14 (original): An electroless plating solution which comprises an aqueous solution containing 0.025 to 0.25 mol/L of a basic compound, 0.03 to 0.15 mol/L of a reducing agent, 0.02 to 0.06 mol/L of copper ion and 0.05 to 0.3 mol/L of tartaric acid or a salt thereof.

15 (original): An electroless plating solution which comprises an aqueous solution containing a basic compound, a reducing agent, copper ion, tartaric acid or a salt thereof and at least one metal ion species selected from the group consisting of nickel ion, cobalt ion and iron ion.

16 (original): The electroless plating solution according to Claim 14 or 15 wherein said electroless plating solution has a specific gravity of 1.02 to 1.10.

17 (currently amended): The electroless plating solution according to any of Claims 14 ~~to 16~~ or 15, the temperature of which is 25 to 40°C.

18 (currently amended): The electroless plating solution according to any of Claims 14 ~~to 17~~ or 15 wherein the copper deposition rate of said electroless plating solution is 1 to 2 μm/hour.

19 (currently amended): An electroless plating process which comprises immersing a substrate in the electroless plating solution according to any of Claims 14 ~~to 17~~ or 15 and performing electroless copper plating at a deposition rate set to 1 to 2 μm/hour.

20 (original): The electroless plating process according to Claim 19 wherein said substrate has a roughened surface.

21 (currently amended): A process for manufacturing a printed circuit board which comprises immersing a resin insulating substrate board in the electroless plating solution according to any of Claims 14 ~~to 17~~ or 15 and performing electroless copper plating at a deposition rate set to 1 to 2 μm/hour to provide a conductor circuit.

Claims 22-26: (canceled).

27 (currently amended): A process for manufacturing a multilayer printed circuit board which comprises at least the following steps (1) to (5)[[.]];

(1) a step for thinning the copper foil of a copper-clad laminate by etching;

(2) a step for piercing through holes in said copper-clad laminate;

(3) a step for depositing a plated metal film on said copper-clad laminate to construct plated-through holes within said through holes;

(4) a step for pattern-etching the copper foil and plated metal film on said copper-clad laminate to construct a conductor circuit; and

(5) a step for serially building up an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit.

28 (original): A process for manufacturing a muitilayer printed circuit board which comprises at least the following steps (1) to (7):

(1) a step for thinning the copper foil of a copper-clad laminate by etching

(2) a step for piercing through holes in said copper-clad laminate

(3) a step for forming a conductor film on said copper-clad laminate

(4) a step of disposing a resist on the area free from conductor circuits and plated-through holes

(5) a step for providing a plated metal film in the resist-free area to construct a conductor circuit and plated-through holes

(6) a step for stripping off said resist and etching the conductor film and copper foil underneath the resist

(7) a step for serially building up an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit.

29 (original): The process for manufacturing a multilayer printed circuit board according to Claim 27 or 28 wherein a laser is used for piercing the through holes in said copper-clad laminate.

30 (original): The process for manufacturing a multilayer printed circuit board according to Claim 27 or 28 wherein a drill is used for piercing the through holes in said copper-clad laminate.

31 (currently amended): The process for manufacturing a multilayer printed circuit board according to any of Claims 27 ~~to 30~~ or 28, wherein, in the step for thinning the copper foil of said copper-clad laminate by etching, the thickness of the copper foil is reduced to 1 to 10 μm.

Claims 32-33: (canceled).

34 (original): A process for manufacturing a multilayer printed circuit board which comprises thinning the copper foil of a copper-clad laminate by etching, pattern-etching the copper foil of said copper-clad laminate to construct a conductor circuit and building up serially an interlayer resin insulating layer and a conductor layer alternately over said conductor circuit wherein the thickness of the conductor circuit on said core board is controlled so as to be not greater by more than 10 μm than the thickness of the conductor layer on said interlayer resin insulating layer.

35 (original): A process for manufacturing a multilayer printed circuit board which comprises constructing an interlayer insulating layer on a substrate formed

with a lower-layer conductor circuit, piercing openings in said interlayer insulating layer, imparting electrical conductivity to the surface of said interlayer insulating layer and the inner walls of said openings, performing electroplating to fill up said openings and thereby provide via holes and, at the same time, construct an upper-layer conductor circuit, wherein said electroplating is performed using an aqueous solution containing a metal ion and 0.1 to 1.5 mmol/L of at least one additive selected from the group consisting of a thiourea, a cyanide and a polyalkylene oxide as a plating solution.

36 (original): The process for manufacturing a multilayer printed circuit board according to Claim 35 wherein the aspect ratio of said openings for via holes, i.e. depth of opening/diameter of opening, is 1/3 to 1/1.

Claims 37 and 38 (canceled).

39 (original): A process for manufacturing a multilayer printed circuit board which comprises at least the following steps (1) to (4):

(1) a step for piercing through holes not larger than 200 μm in diameter in a core board by laser

(2) a step for plating said through holes therein to construct plated-through holes

(3) a step for constructing an interlayer resin insulating layer provided with openings communicating with said plated-through holes on the core board

(4) a step for plating the openings in said interlayer resin insulating layer to construct via holes in the manner of plugging the through holes in said plated-through holes.

Claims 40-46 are cancelled.

47 (new): The process for manufacturing a multilayer printed circuit board according to claim 28, wherein, in the step for thinning the copper foil of said copper-clad laminate by etching, the thickness of the copper foil is reduced to 1 to 10 μm.